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IMMORTAL

Integrated Modelling, Fault Management, Verification and Reliable Design Environment for Cyber-Physical Systems

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Integrated FPGA demonstrator of the fault management framework
(Deliverable D5.2)

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v. 1.00

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Public, fully open

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Classified
Notices

For information on this deliverable, please contact e-mail: info@h2020-immortal.eu. This document is intended to fulfil the contractual obligations of the IMMORTAL project concerning Deliverable D4.4 described in contract 644905.

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About

This document is the report for demonstrator Deliverable D5.2 (“Integrated FPGA demonstrator of fault management framework”) of Workpackage WP5 (“Demonstration”) of the H2020 RIA IMMORTAL.
## List of Abbreviations

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<th>Description</th>
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<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
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<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
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<td>HM</td>
<td>Health Monitor</td>
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<td>HW</td>
<td>Hardware</td>
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<tr>
<td>IJTAG</td>
<td>Internal JTAG standard (IEEE 1687, iJTAG)</td>
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<tr>
<td>IP</td>
<td>Intellectual Property</td>
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<tr>
<td>NoC</td>
<td>Network-on-Chip</td>
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<td>SoC</td>
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Executive Summary

This demonstrator shows how to immortalize a subsystem IP using the fault management infrastructure devised in the IMMORTAL project. The result is a systematic and efficient approach to add fault management HW and SW infrastructure to a subsystem IP integrated into a SoC. This demonstrator applies and extends the IMMORTAL ASIC demonstrator by integrating the IMMORTALIZED NoC IP into a multicore processing subsystem IP.

The demonstrator is built in seven steps. Given a NoC-based multicore processing subsystem IP, the following steps are executed.

1. Add Health Monitors (HMs)
2. Add IJTAG network connecting HMs
3. Create IJTAG network specification table
4. Add Instrument Manager
5. Integrate immortalized subsystem into the SoC
6. Add Instrument Manager driver SW
7. Integrate with system SW

Using these steps the technologies developed and prototyped in WP4 are stepwise applied to create an integrated IMMORTALIZED subsystem. Hereafter, the multicore SoC has an immortalized subsystem for which application and subsystem specific SW can be written using the IMMORTAL framework to monitor and configure the subsystem. The resulting SoC is implemented on a Xilinx Zynq-7000 platform.

To illustrate the features of the created system, we provide a simple application example and show how to monitor and reconfigure the system.